

## DATA PROCESSING SYSTEM AND METHOD

### ABSTRACT

5 A powerful, scaleable, and reconfigurable image processing system and method of processing  
data therein is described. This general purpose, reconfigurable engine with toroidal topology,  
distributed memory, and wide bandwidth I/O are capable of solving real applications at real-time  
speeds. The reconfigurable image processing system can be optimized to efficiently perform  
specialized computations, such as real-time video and audio processing. This reconfigurable image  
processing system provides high performance via high computational density, high memory  
bandwidth, and high I/O bandwidth. Generally, the reconfigurable image processing system and its  
control structure include a homogeneous array of 16 field programmable gate arrays (FPGA) and 16  
static random access memories (SRAM) arranged in a partial torus configuration. The reconfigurable  
image processing system also includes a PCI bus interface chip, a clock control chip, and a datapath  
chip. It can be implemented in a single board. It receives data from its external environment,  
15 computes correspondence, and uses the results of the correspondence computations for various post-  
processing industrial applications. The reconfigurable image processing system determines  
correspondence by using non-parametric local transforms followed by correlation. These non-  
parametric local transforms include the census and rank transforms. Other embodiments involve a  
combination of correspondence, rectification, a left-right consistency check, and the application of an  
20 interest operator.